Iraqi Journal of Industrial Research, Vol. 11, No. 1 (2024)

Open Access

Iraqi Journal of Industrial Research (IJOIR)

Journal homepage: http://ijoir.gov.iq

VLSI Synthesis for Low-Power Clocking in Synchronous Designs

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Article information

Article history:
Received: November, 22, 2023
Accepted: February, 08, 2024
Available online: June, 14, 2024

Keywords:
ALU Circuit,
Clock Gating Technique,
Optimization of Parameters

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DOI:
https://doi.org/10.53523/ijoirVol11I1ID423

Abstract

In the field of information theory, the significance of low-power techniques cannot be overstated. Among these, clock gating stands out as a potent method to mitigate power dissipation in synchronous designs. The landscape has been further shaped by VLSI innovations, which, in their initial stages, necessitated substantial equipment, incurred high power consumption, and exhibited occasional unreliability. This paper explores the evolution from these challenges to a paradigm where advancements in VLSI technology have resulted in smaller, more affordable, reliable, and power-efficient systems. Focusing on the Arithmetic Logical Unit (ALU) design, our study presents a comparative analysis of power consumption across various existing clock gating techniques. Introducing an innovative signal clock gating method, we address contemporary challenges with an accessible mechanism, enhancing immunity. Our proposed Gated Clock Generation design, employing a tri-state connection and logic gate, demonstrates superior power savings, even when applied to the target module. This approach optimizes power efficiency in digital design while proving particularly effective in reducing dynamic power within logic circuits. Implementing an improved gate-based clock gating technique in ALU design, our results show a noteworthy reduction in clock delay (71% to 78%), a 23% improvement in area, and a substantial 66.67% enhancement in power efficiency. Notably, this clock gating scheme surpasses alternative methods in terms of area requirements. The experiments, exclusively conducted on ALU design, utilized 130 nm standard logic libraries for implementation. The design architecture was meticulously crafted using Verilog HDL, and simulations were executed with ModelSim-Altera 10.0c (Quartus II 11.1) Starter Version.

1. Introduction

Recently larger and more efficient batteries are being used to solve excessive power consumption problem. Therefore, in the modern days economic and environmental issues have forced the researchers to think on improvement and proffer solutions for reducing power consumption and increasing reliability in digital systems. This work was developed in relation with Synopsys and it aims at studying, practicing and evaluating digital design

techniques for data compression and minimization of power consumption through flexibility of design. This aim is achieved in modern design with the use of high-speed digital interface.

Nowadays, VLSI plays a significant role in a variety of applications, including robotics, DSP, RF, low power, networks, microwave applications, MEMS, and space applications. A process to create integrated circuits microchips by combining figures of 1000s of transistors or logic blocks on a single chip is called VLSI system design. A circuit of electronics consists of elements, which are the fundamental components of a digital system and can be a transistor, diode, or resistors coupled in a certain way to carry out a logic function known as a gate circuit [1], [2]. In VLSI digital design, there are three primary criteria to consider: power, area, and delay. This study discusses dynamic power reduction in an 8-bit ALU circuit. Generally speaking, electronic systems and integrated circuits in particular have higher power consumption due to their complexity stemming from the large number of circuits on a single chip. Thus, it is necessary to build a circuit that uses less power [3].

2. Power Dissipation

The power defined as the amount of energy is delivered to the circuit. Power dissipation is explained as the process of the rate of electric energy transferred in terms of heat energy. The process of optimizing is explained in terms of creating the ideal design for the intended use. Three main sources of power dissipation are explored while building VLSI systems: Short-circuit power, static power, and dynamic power, sometimes known as circuit-switching power. As seen in Figure (1), dynamic power is a very basic method for estimating the amount of energy consumed in a CMOS circuit. Switching activities in the circuit are what induce the dynamic power. Higher operating frequencies are used in the system to increase dynamic power, which causes the circuit to turn on more frequently [4]]. The particular expression describes the dynamic power of the presented circuit, where the capacitance to stay switched in CMOS circuits projects energy consumption. In VLSI circuits, capacitance charging and discharging are recognized as the primary source of dynamic power dissipation [5].

$$\boldsymbol{P} = \propto C\ F\ V^2 \qquad \textbf{(1)}$$

Since static power is associated with the states of the used circuits, it can be inferred that, instead of switching activities as seen in Figure (2), static power results from the changing of circuit states that are 0 to 1 or 1 to 0. Leakage power is the only source of static power dissipation in CMOS circuits. In digital CMOS technology, low power consideration needs to be applied at all design abstraction and design activity levels. Reliability, design cycle time, testability, and design complexity are among the other characteristics that are impacted by low-power design systems. The two main trade-offs taken into account while building a VLSI system are chip area and speed [6], [7].

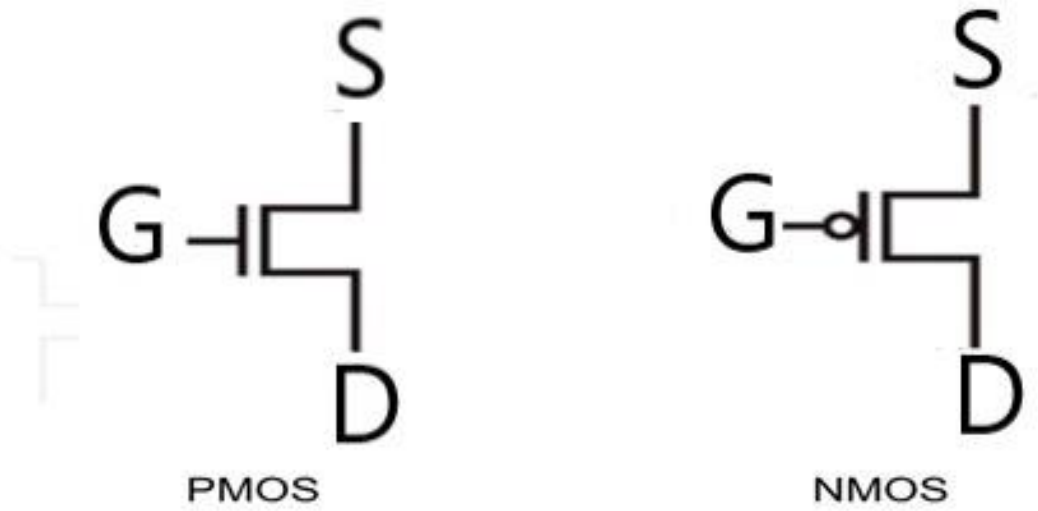

Figure (1): Switching power.

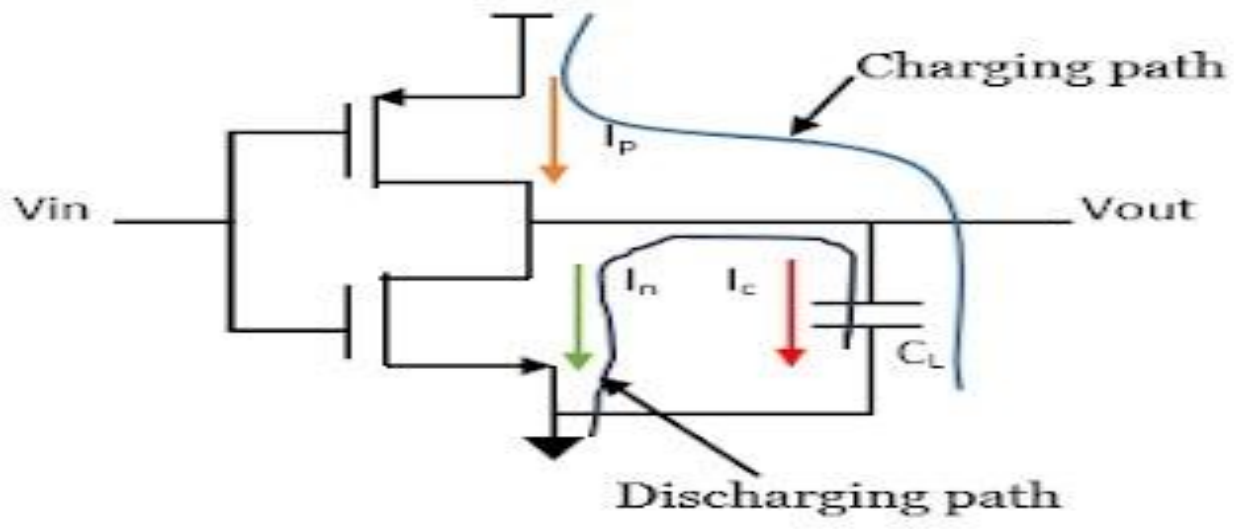

Figure (2): Static (leakage) Power.

3. Problem Formulation

As part of earlier research, various designs for low-power VLSI systems were investigated. The clock gating technique is used in this paper to design an ALU circuit. Clock gating is a popular technique to reduce power dissipation in clock circuits. Clock gating saves more power to adding more logic to the clock circuitry [8]The internal clock of a clock CMOS circuit utilizes some of the clock energy, as well as buffers are applied to control the transaction gates. With clock gating design the difference is that the gating function is derived within the circuit without an external control signal. Clock gating technique switch the design on just the target module that's need to take the output. In order to use and benefit from clock-gating, a design must be contain these enable conditions [9]The clock signal is derived to the resistors only when EN is 1, so power consumption is reduced which is related to the switching activity of the clock. Therefore, clock gating technique is widely used technique for dynamic power reduction in digital CMOS IC circuits [10]. Clock gating is achieved with Flip-flops, latches, AND/OR gate in the clock signal and a control signal to construct of gated clock signal, then be relevant to distinct components of the circuit. Exception to Power, there are two other parameters also optimized in an 8-bit ALU circuit i.e., Area and Delay are reduced with Clock delay [11], [12].

4. Proposed System

The paper described the clock gating approach, which is employed in the 8-bit ALU circuit to achieve low power dissipation. The circuit is designed with clock gating techniques [13]. The ALU block has a very important role in IC design for the computation of arithmetical and digital operations. ALU is regarded as an arithmetic unit, a logic unit, and output multiplexers in a block. Using input registers, data is loaded into the arithmetic and logical units, and the output is sent to an output register. The gated clock controlled the data in the registers from the clock gating circuitry. This article reviewed all related research involving the clock gating technique. Also, here two types of clock gating techniques were used to propose the design of ALU, notably AND gate-based clock gating and XOR gate-based clock gating technique and then comparing their results for area analysis of the circuit.

5. A New Technology for Clock Gating

This work built a new circuit designed to save more power. In order to accomplish this, the connected bubbling input NAND gate and the tri-state buffer connection are used to create the new Gated Clock signal that is depicted in Figure (3). This function maintains power even in the event that the target device's clock is on, the controlling device's clock is off, or both are off. By avoiding needless clock signal switching, the objective design will reduce the amount of power needed in these operations.

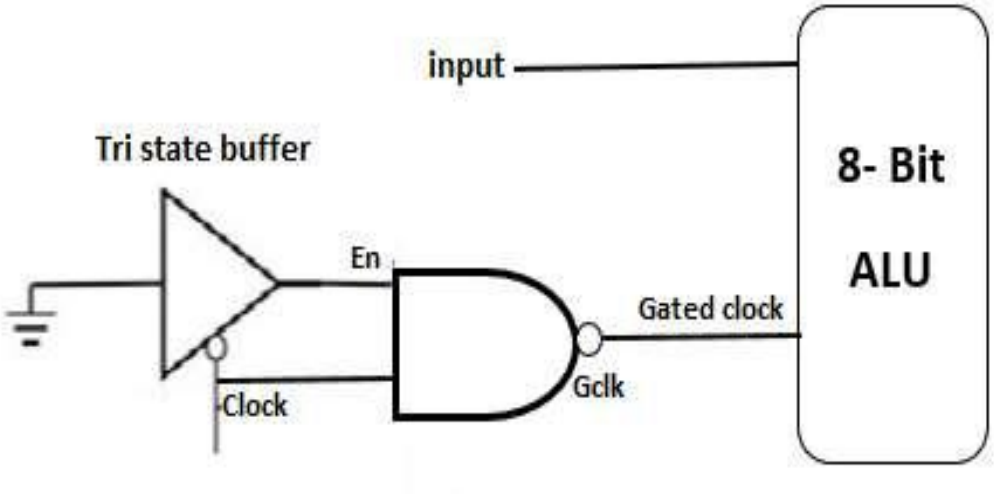

Figure (3): Proposed Clock Gating.

The input signal called Clk is supplied to the NAND and tri-state buffer connection. Basically, whenever the clock switches to 1, En is 0 in this state output, and output 1 will be generated by NAND logic with neg-edge clock, and this output value goes to the first generation of the clock that generates the signal used for design control. The logic of the tri-state was the first logic, having the Global Clock as an input at the other ground input. As x switches to 1, this relation will generate a clock signal used to monitor the latch. In the next cycle, when the clock flips to 0, the logic of the second clock generation is a NAND gate with En and Global Clk at its input and generates a clock pulse that goes to the target unit when Gen goes '1'. Since GEN is 1 the NAND generates 1 so OR generates constant HIGH at CClk (Composite Clock) until En turns to 0. GClk (Global Clock) will be running this way and CClk will be at Constant 1 mode, which ensures that without any switching the latch will keep its state. To understand the working of the circuit for all process steps. A Tri-state Buffer can be thought of as an input-controlled switch with an output that can be electronically turned ON or OFF by means of an external Control or Enable (EN) signal input. This control signal can be either a logic 0 or a logic 1 type signal resulting in the Tri-state Buffer being in one state allowing its output to operate normally producing the required output or in another state where its output is blocked or disconnected. Then a tri-state buffer requires two inputs. One being the data input and the other being the enable or control input. When activated into its third state it disables or turns OFF its output producing an open circuit condition that is neither at a logic HIGH or LOW, but instead gives an output state of very high impedance, High-Z, or more commonly Hi-Z. This type of device has two logic state inputs, 0 or a 1 but can produce three different output states, 0, 1 or Hi-Z which is why it is called a Tri or 3-state device.

6. ALU Circuit

ALU has been designed to perform operations of addition, subtraction, multiplication, shift operations and logical operations. We have implemented the following 8 functions using ALU:

6.1. Arithmetic Unit

The four types of arithmetic operations that can be performed by an arithmetic unit are addition, subtraction, increment, and decrement. ALU takes into account 8-bit inputs A and B and carries input. Carry input is used to apply inputs A and B through registers. The gated clock signal again from the clock gating circuit controls A and B by registers. As a result, the arithmetic unit only performs operations when necessary while the other ones are inactive. Table (1) is used to display operations carried out by the arithmetic unit of the ALU [14]

Table. (1). Operations Performed in ALU.

A	B	C_{IN}	Operation
0	0	0	A+B
0	0	1	A-B
0	1	0	NOT
0	1	1	A NAND B
1	0	0	A NOR B
1	0	1	A AND B
1	1	0	A OR B
1	1	1	A XOR B

6.2. Logic Unit

To carry out logical operations, the operands A and B enter the logic unit by a regulated signal generated by the gated clock. Operations performed in the logic unit are shown in tabular form below. There are AND, NAND, NOR, and XOR operations performed by arithmetic logical units [15].

Table (2). Operations Performed in Logic Unit

A	B	Operation
0	0	AND
0	1	NAND
1	0	NOR
1	1	XOR

7. Experimental Analysis

The Verilog HDL is utilized for the development of the ALU design architecture and ModelSim-Altera 10.0c (Quartus II 11.1) is used to carry out the simulations. Figure (4) presents the implementations of an 8-bit ALU circuit coded in Verilog HDL utilizing the clock-gating technique, which uses AND gates and XOR gates.

8. Results and Discussion

In this section the results of the dissertation are presented in the form of a table showing delay, area and power for various combinations of experiments carried out. The simulation performed simulations are performed utilizing ModelSim-Altera 10.0c (Quartus II 11.1) Starter Version of ALU circuit without using Clock Gating in Figure (4), and with using Clock Gating in Figure (5).

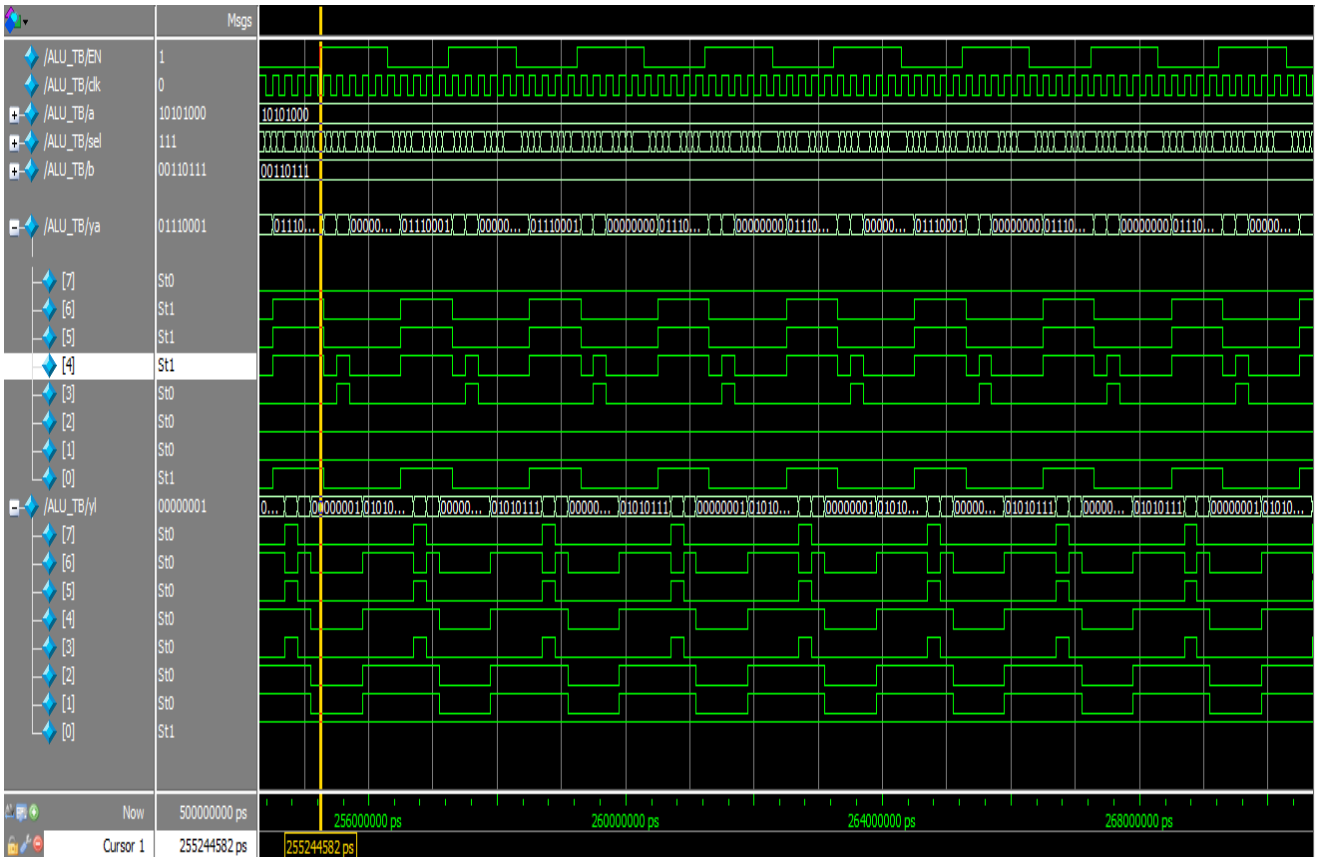

Figure (4): Simulation results without Clock gating concept.

There are timing diagrams and synthesis reports generated after the simulation of the projected system, which are referred as simulation results and help to calculated Delay and Area of the circuit.

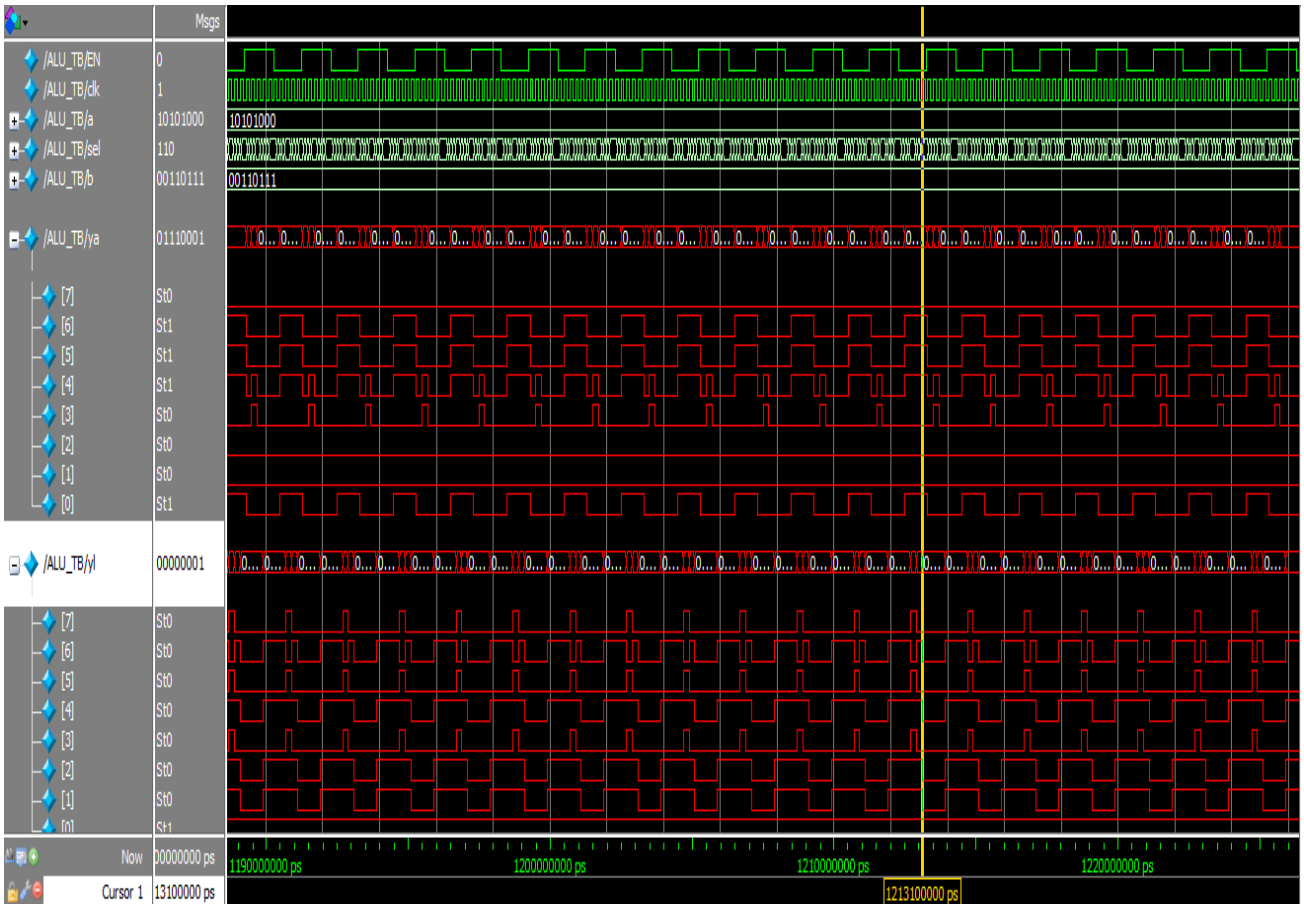

Figure (5): Simulation results with Clock Gating concept.

8.1. Optimizing Delay Using Clock Gating

Table (3) shows the optimization of the delay in the investigated circuit is achieved with the help of the synthesis information. Consequently, the gate delay as well as net delay using circuit interconnected system describe the delay at the logic levels of such circuit [16]

Table (3): Delay Reduction with Clock Gating.

Parameter		**Value**	
Logic Levels		**Without Clock Gating**	**With Clock Gating**
Logic level 1	Gate delay	6.102 ns	1.064 ns
	Net delay	2.789 ns	0.811 ns
Logic level 2	Gate delay	6.863 ns	0.361 ns
	Net delay	0.420 ns	0.279 ns
Logic level 3	Gate delay	---	0.098 ns
	Net delay	---	0.696 ns

8.2. Area Optimization in ALU with Clock Gating

With the synthesis report optimization of the area in the circuit is obtained and shown in Table (4). Input-output ports, flip-flops, multiplexers, and overall memory usage are all examples of components that are defined as part

of the area optimization concept [17] with using Clock gating concept always area will always be increased due to added external circuitry of the clock network. The findings of this comparison between AND gate and XOR gate-based clock gating are displayed in Table (4), where an area is reduced in the XOR gate-based clock gating approach. As you can see in (Total memory used) section that the XOR gate less than AND gate.

Table (4): Area Reduction with Clock Gating.

Device summary	Without Clock Gating	AND gate-based clock gating	XOR gate-based clock gating
No. of I/O	28	30	30
No. of Bells	80	32	32
No. of LUTs	88	17	17
Input Buffers	19	21	21
Output Buffers	8	9	9
Clock - Buffers	1	0	0
No. of MUXs.	31	7	7
No. of Flops / latches	16	16	16
Total memory used	253832 k bytes	328580 k bytes	257736 k bytes

8.3. Power Optimization in ALU with Clock Gating

With the synthesis report optimization of area in the circuit is obtained and shown in Table (5) as given below, here dynamic power is calculated by the simulation and the result shows that the power is minimized in the ALU with the proposed technique.

Table (5): Power Reduction with Clock Gating.

Power Synthesis in ALU Circuit with Clock Gating technique		
Dynamic Power oforiginal ALU circuit	Dynamic Power of Clock Gated ALU circuit	Total Power Reduction in ALU circuit using Clock Gating
6.236 kilo watts	2.234 kilo watts	66.67%

The design of an 8-bit ALU circuit is examined at different input vectors by using a simulating tool [18] in Figures (4 & 5), the observed results are graphically explained. Results have demonstrated that applying clock gating in an 8-bit ALU circuit reduces delay by 70% to 75% and power consumption by 66.67%. Thus, the clock Gating technique achieves significant reduction in the delay and power [19] Also, there is area reduction will be achieved with a reduction in a number of stages.

Results of Power and Area in comparison to AND and XOR gate-based clock gating technique show that 50% to 70% of power reduction is achievable with AND gate-based clock gating technique while 66.7% of power reduction is attainable with XOR gate-based clock gating technique. Area increases when using the AND gate-based clock-gating technique because of external clock-gating circuitry, which can be decreased 21.56% when using the XOR gate-based clock-gating technique.

9. Conclusion

Finally, a new technology of ALU design that saves more power, the Clock Gating technique for reducing delay and dynamic power is taken into consideration. An 8-bit ALU circuit that uses the Clock Gating approach has been constructed, and the results are better. The main contribution of this research is to develop a new tri-state buffer connection with clock gating and enhanced design efficiency. The main idea of this research is that the design deals with new gate design as a switch not register, because the register consume much power. Therefore, reducing switching operation prevents these constraints from being prevented by the design. With low power dissipation, a new design of tri-state connection-based clock gating was successfully synthesized and analyzed. The additional clock skewing, however, might be less for maximum operation frequency. The behavioral characteristics of a clock were examined based on its triggering action. The developed gated clock signal in this paper has the ability to decrease power dissipation in the circuit, according to behavior circuit modeling. Also, results of comparisons between XOR gate-based clock gating along with AND gate-based clock gating are displayed.

Conflict of Interest: The authors declare that there are no conflicts of interest associated with this research project. We have no financial or personal relationships that could potentially bias our work or influence the interpretation of the results.

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